FIG. 1 (PRIOR ART)

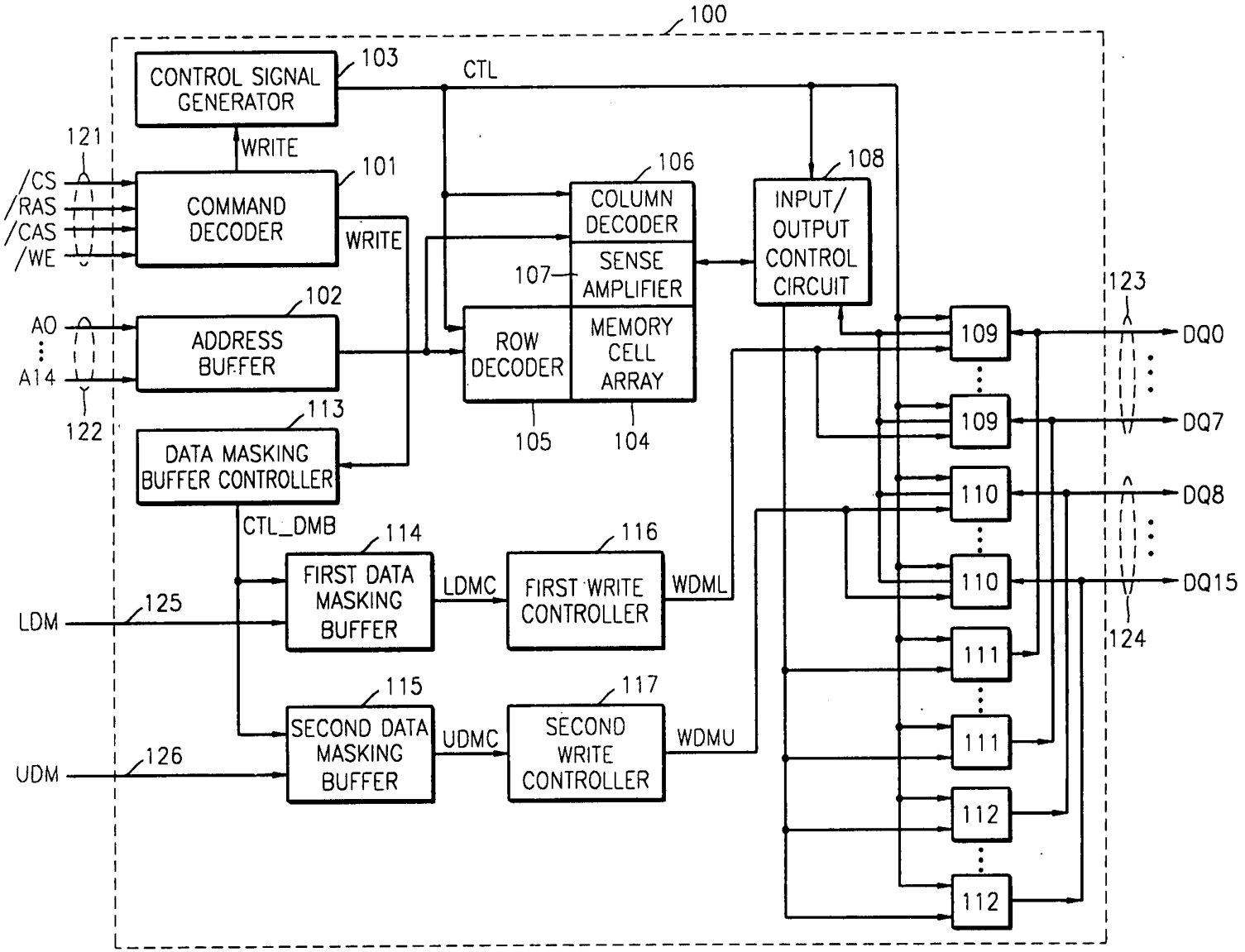


FIG. 2 (PRIOR ART)

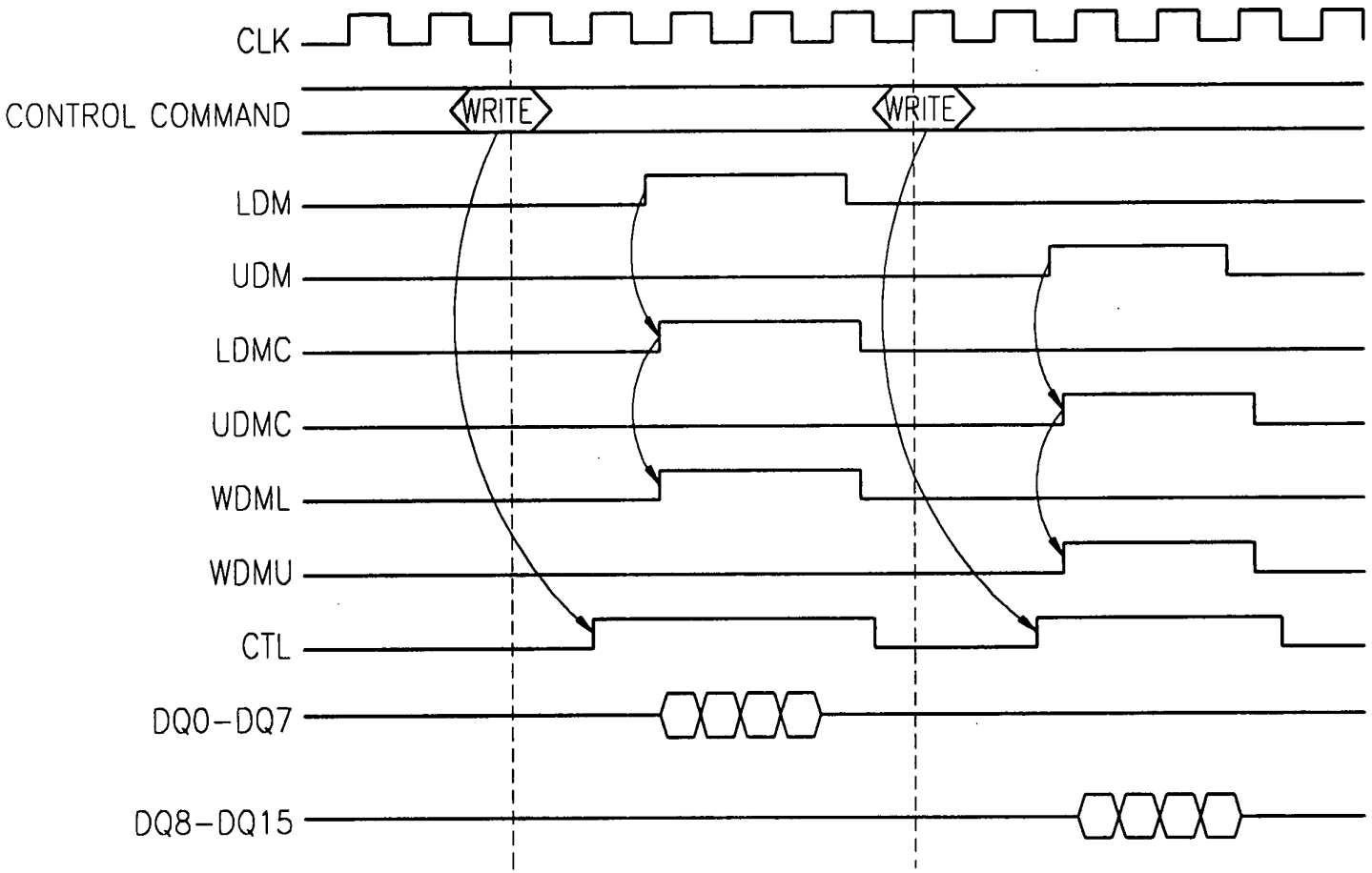


FIG. 3

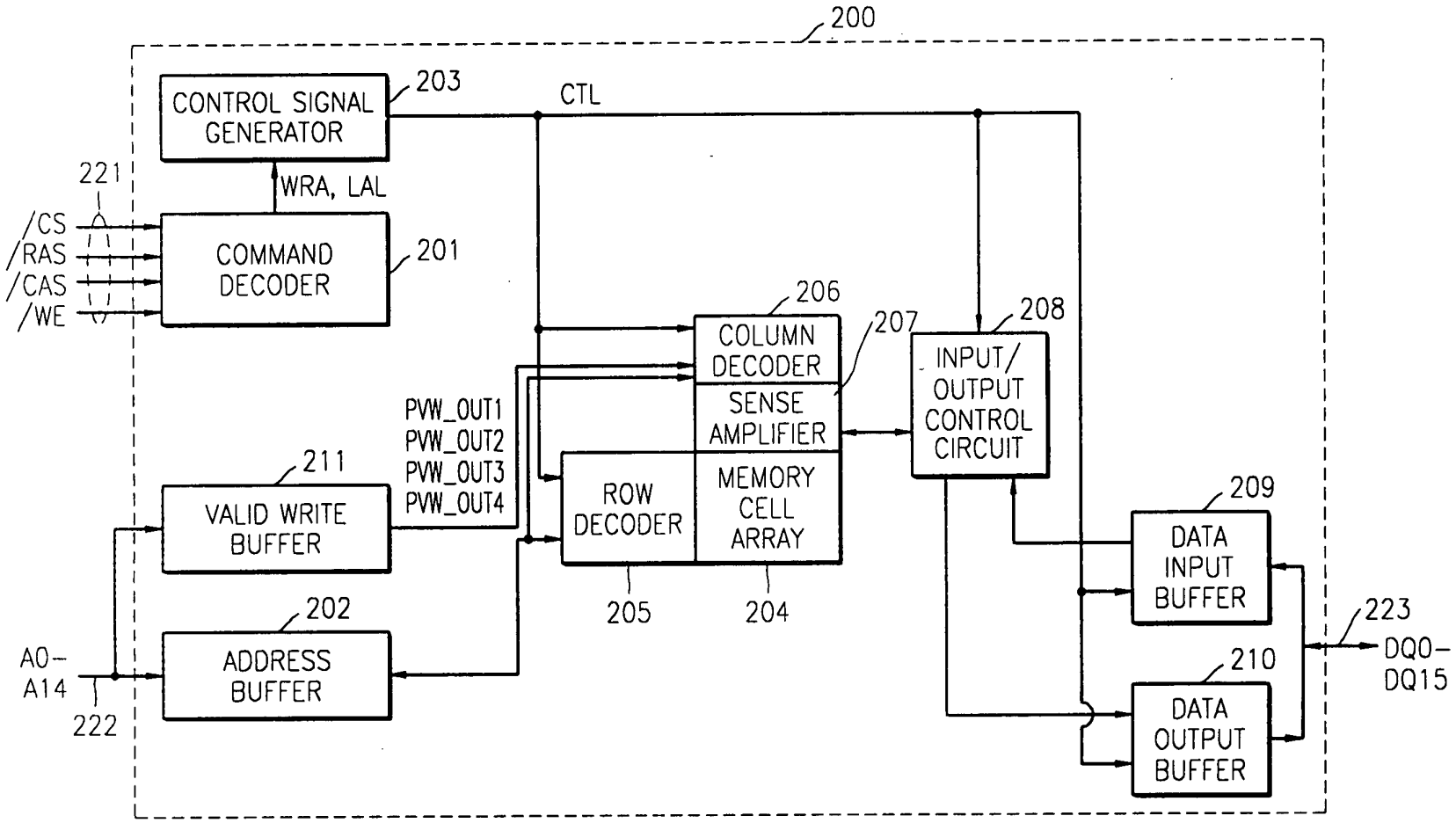

200
CONTROL SIGNAL GENERATOR
203
CTL
WRA, LAL
221
/CS
/RAS
/CAS
/WE
COMMAND DECODER
201
206
COLUMN DECODER
207
208
SENSE AMPLIFIER
INPUT/ OUTPUT CONTROL CIRCUIT
PVW_OUT1
PVW_OUT2
PVW_OUT3
PVW_OUT4
211
VALID WRITE BUFFER
ROW DECODER
MEMORY CELL ARRAY
205
204
209
DATA INPUT BUFFER
223
DQ0-
DQ15
202
A0-
A14
222
ADDRESS BUFFER
210
DATA OUTPUT BUFFER

FIG. 4

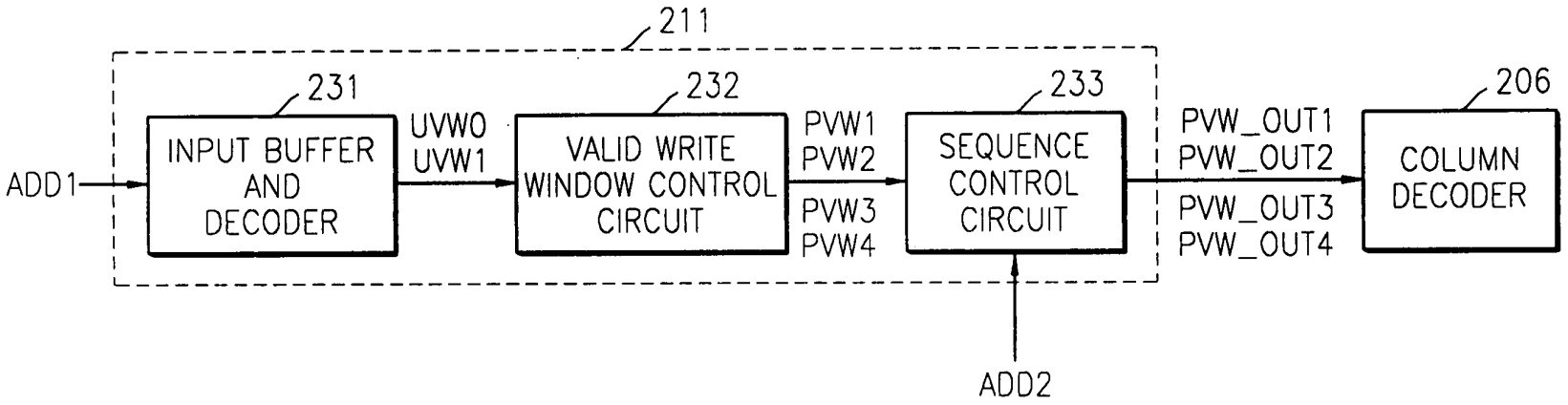

211
231
INPUT BUFFER AND DECODER
ADD1
UVW0
UVW1
232
VALID WRITE WINDOW CONTROL CIRCUIT
PVW1
PVW2
PVW3
PVW4
233
SEQUENCE CONTROL CIRCUIT
ADD2
PVW_OUT1
PVW_OUT2
PVW_OUT3
PVW_OUT4
206
COLUMN DECODER

FIG. 5

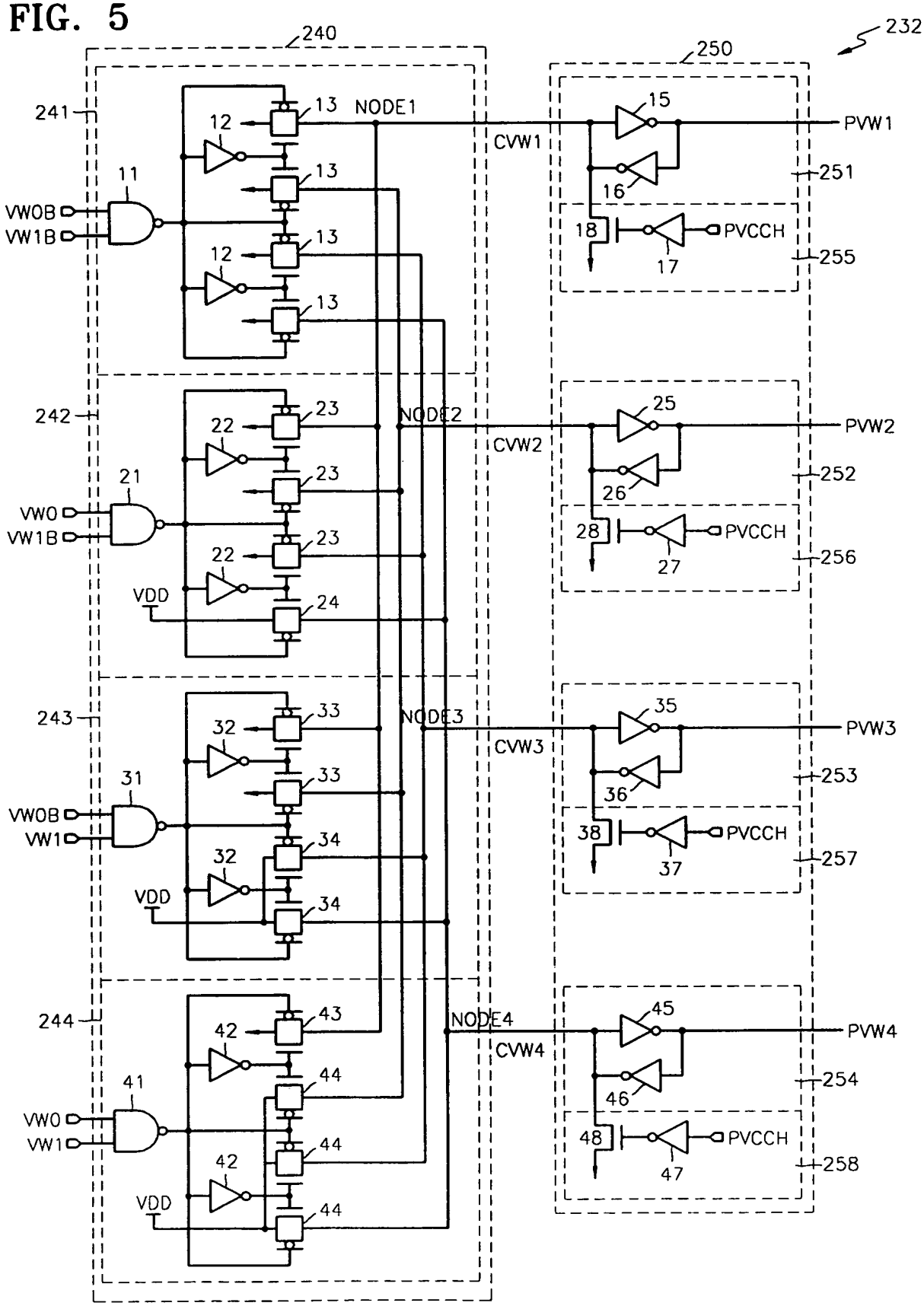

240
250
232
241
242
243
244
NODE1
NODE2
NODE3
NODE4
CVW1
CVW2
CVW3
CVW4
PVW1
PVW2
PVW3
PVW4
VW0B
VW1B
VW0
VW1
VDD
PVCCH
11
12
13
15
16
17
18
21
22
23
24
25
26
27
28
31
32
33
34
35
36
37
38
41
42
43
44
45
46
47
48
251
252
253
254
255
256
257
258

FIG. 6

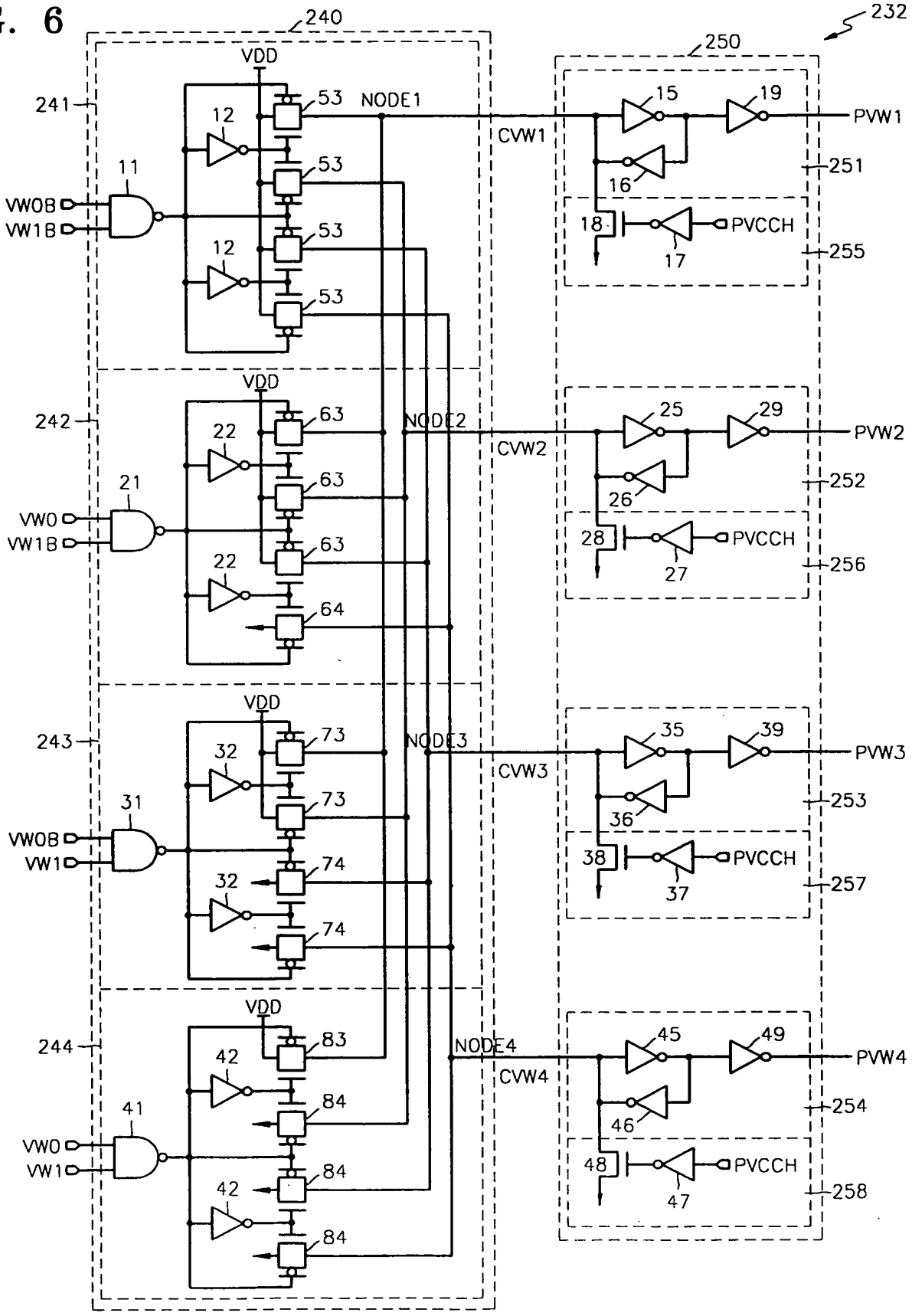

232
240
250
VDD
241
242
243
244
NODE1
NODE2
NODE3
NODE4
CVW1
CVW2
CVW3
CVW4
PVW1
PVW2
PVW3
PVW4
VW0B
VW1B
VW0
VW1
PVCCH
11
12
21
22
31
32
41
42
15
16
17
18
19
25
26
27
28
29
35
36
37
38
39
45
46
47
48
49
251
252
253
254
255
256
257
258

FIG. 7

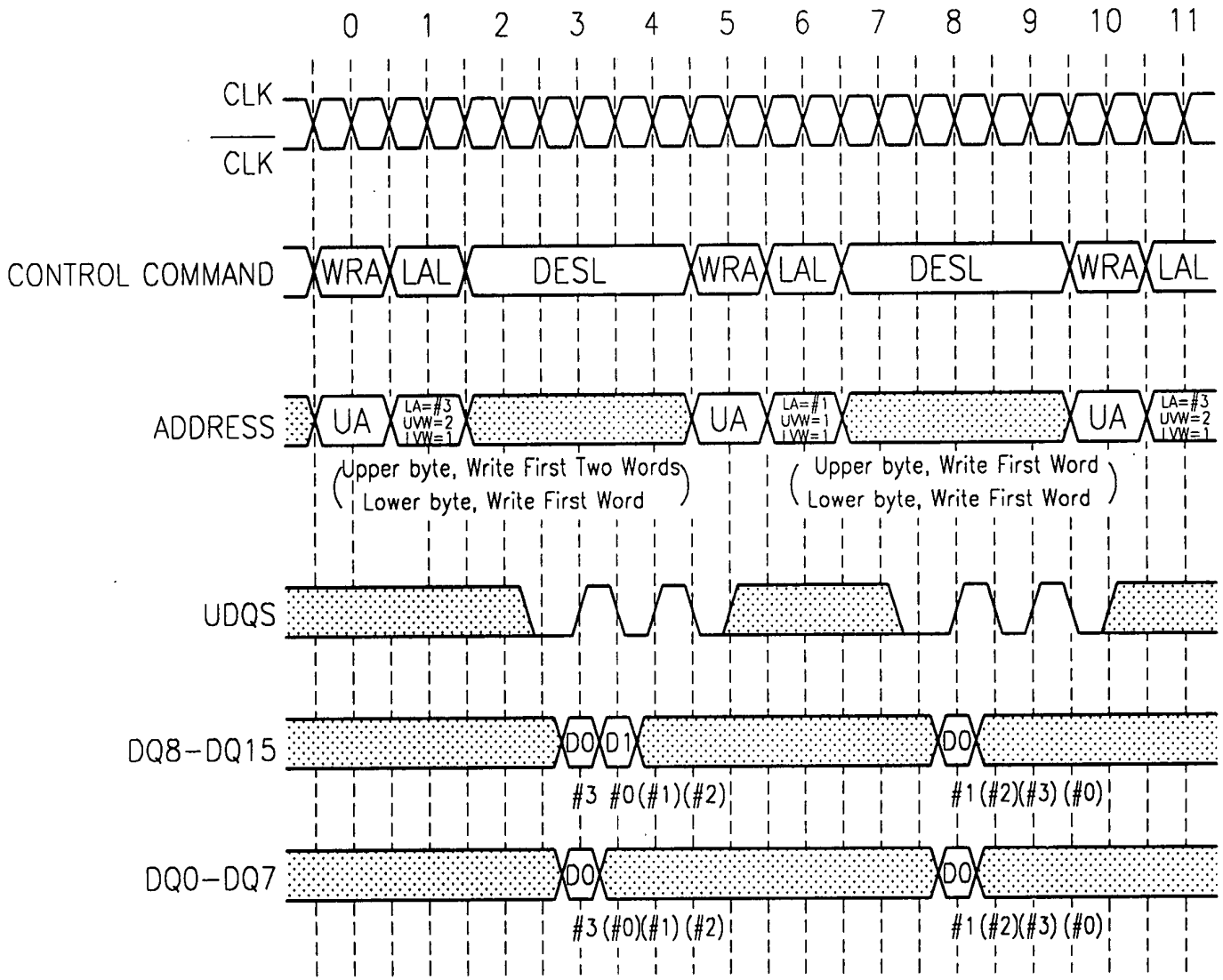

0
1
2
3
4
5
6
7
8
9
10
11
CLK
CLK
CONTROL COMMAND
WRA
LAL
DESL
WRA
LAL
DESL
WRA
LAL
ADDRESS
UA
LA=#3
UVW=2
LVW=1
UA
LA=#1
UVW=1
LVW=1
UA
LA=#3
UVW=2
LVW=1
Upper byte, Write First Two Words
Lower byte, Write First Word
Upper byte, Write First Word
Lower byte, Write First Word
UDQS
DQ8-DQ15
D0
D1
D0
#3 #0(#1)(#2)
#1(#2)(#3)(#0)
DQ0-DQ7
D0
D0
#3(#0)(#1)(#2)
#1(#2)(#3)(#0)

FIG. 8

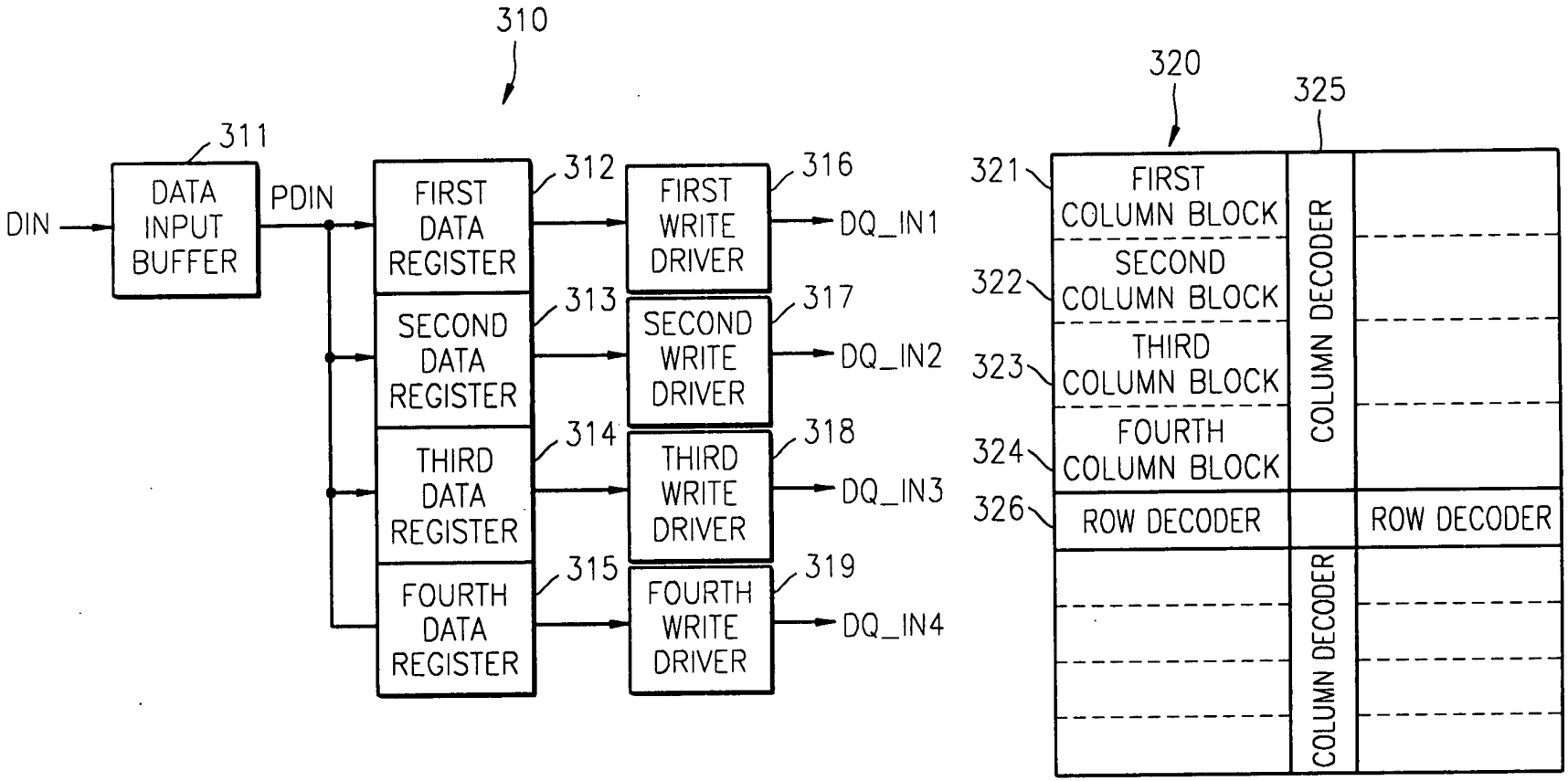

310
311
DATA INPUT BUFFER
DIN
PDIN
FIRST DATA REGISTER
SECOND DATA REGISTER
THIRD DATA REGISTER
FOURTH DATA REGISTER
312
313
314
315
FIRST WRITE DRIVER
SECOND WRITE DRIVER
THIRD WRITE DRIVER
FOURTH WRITE DRIVER
316
317
318
319
DQ_IN1
DQ_IN2
DQ_IN3
DQ_IN4
320
325
321
322
323
324
326
FIRST COLUMN BLOCK
SECOND COLUMN BLOCK
THIRD COLUMN BLOCK
FOURTH COLUMN BLOCK
COLUMN DECODER
ROW DECODER
ROW DECODER
COLUMN DECODER

FIG. 9

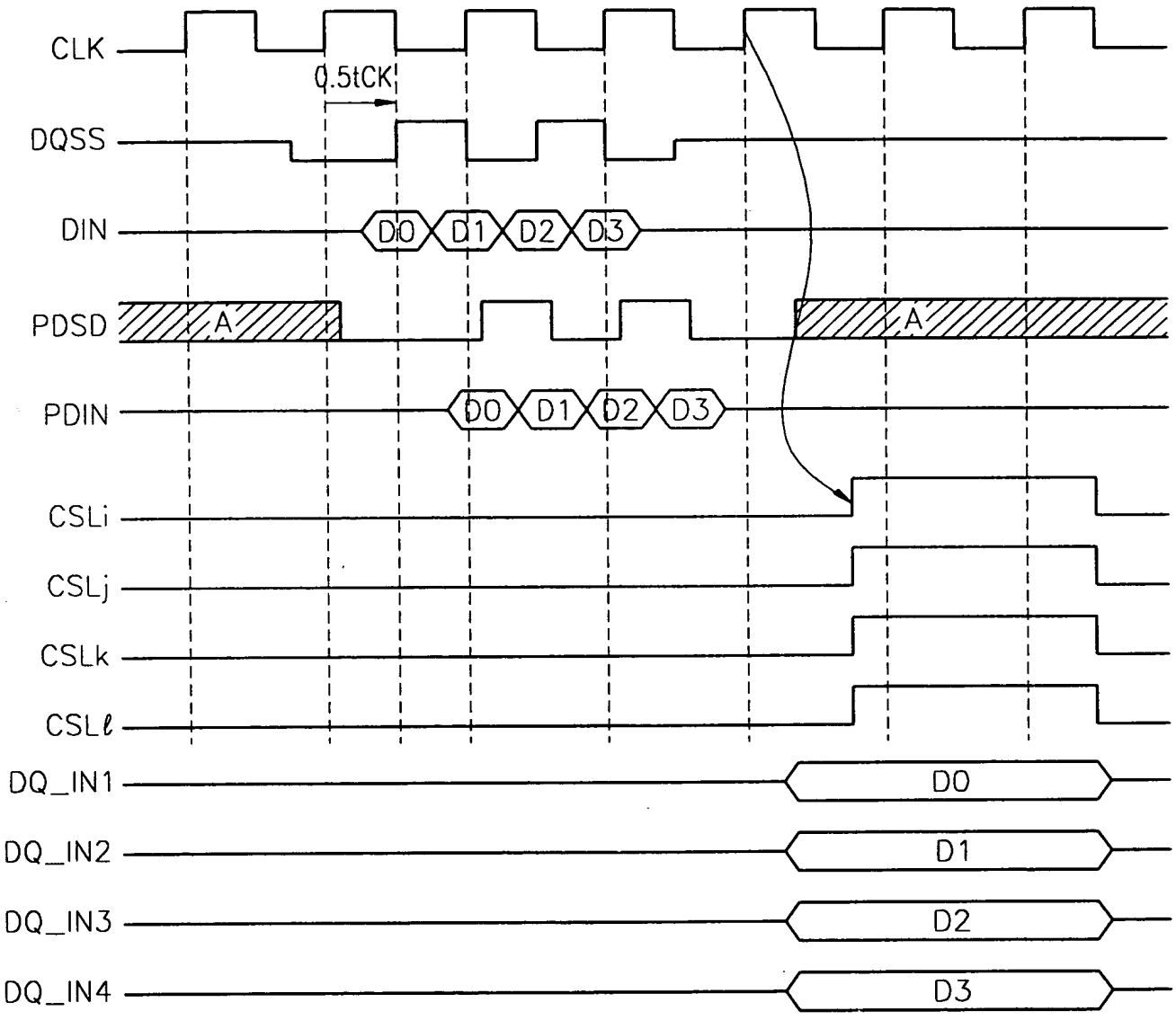

CLK
0.5tCK
DQSS
DIN
D0
D1
D2
D3
PDSD
A
A
PDIN
D0
D1
D2
D3
CSLi
CSLj
CSLk
CSLℓ
DQ_IN1
D0
DQ_IN2
D1
DQ_IN3
D2
DQ_IN4
D3

FIG. 10

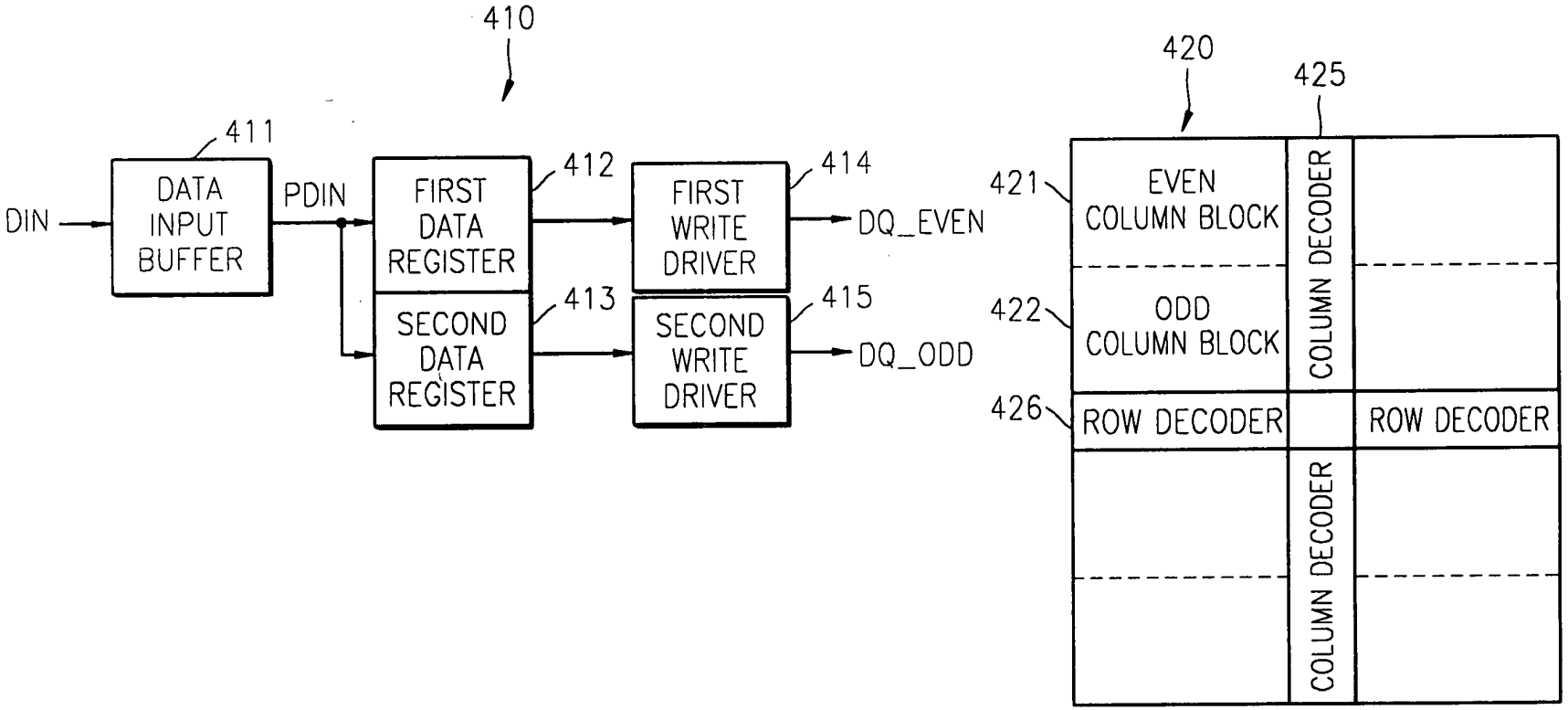

410
411
DIN
DATA INPUT BUFFER
PDIN
FIRST DATA REGISTER
412
SECOND DATA REGISTER
413
FIRST WRITE DRIVER
414
DQ_EVEN
SECOND WRITE DRIVER
415
DQ_ODD
420
425
421
EVEN COLUMN BLOCK
422
ODD COLUMN BLOCK
426
ROW DECODER
ROW DECODER
COLUMN DECODER
COLUMN DECODER

FIG. 11

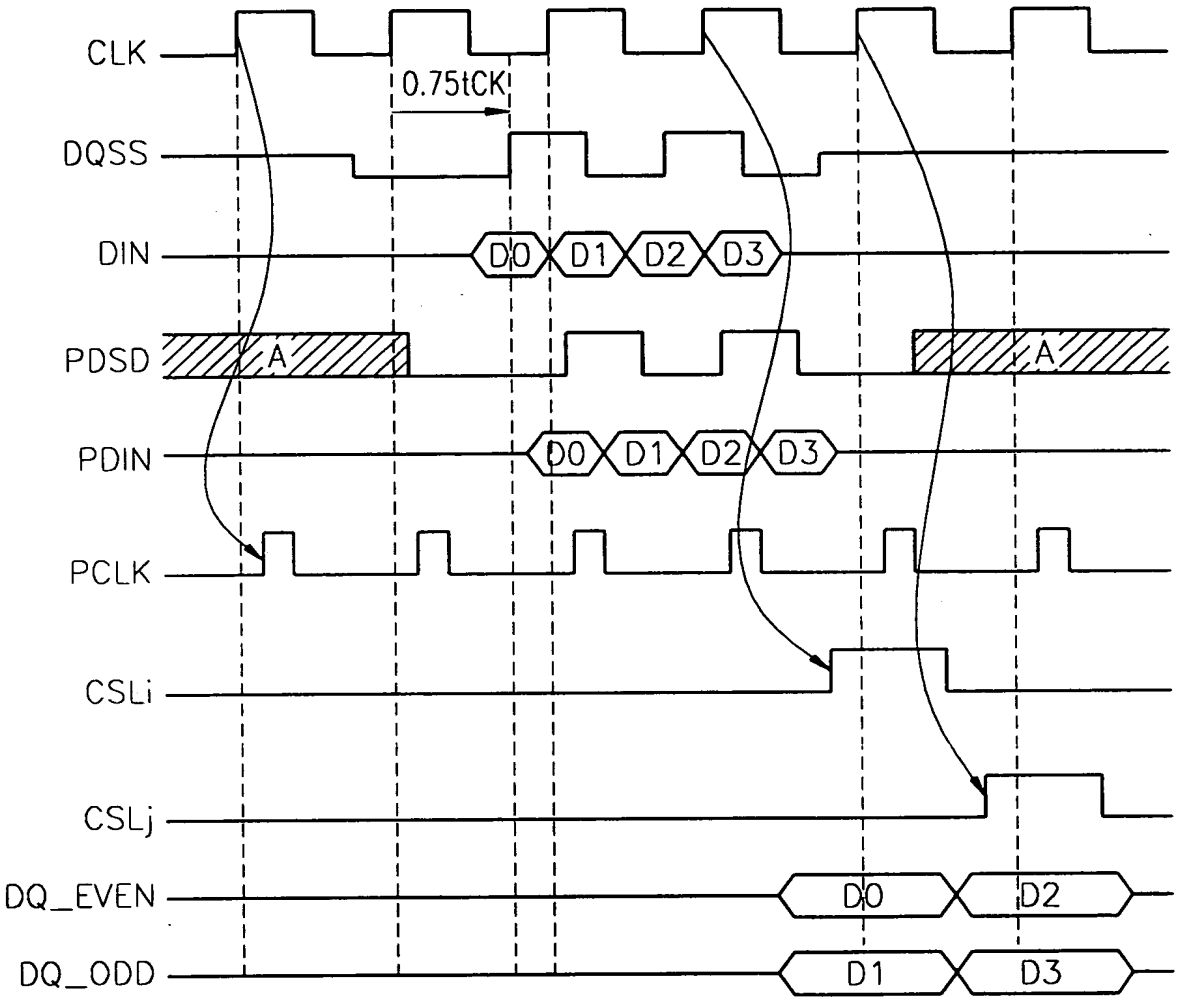
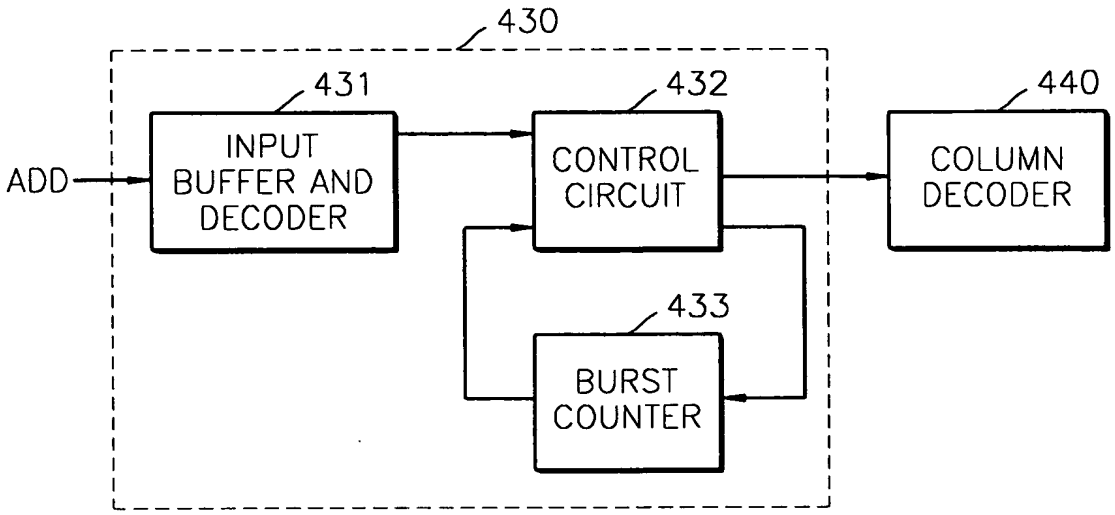

CLK
0.75tCK
DQSS
DIN
D0
D1
D2
D3
PDSD
A
A
PDIN
D0
D1
D2
D3
PCLK
CSLi
CSLj
DQ_EVEN
D0
D2
DQ_ODD
D1
D3

FIG. 12


430
431
INPUT BUFFER AND DECODER
ADD
432
CONTROL CIRCUIT
433
BURST COUNTER
440
COLUMN DECODER